Remarks

Applicant respectfully requests reconsideration of this application as amended. Claims 1, 7, 10, 18, and 21 have been amended. Claims 6, 17, and 28 have been cancelled. No claims have been added. Therefore, claims 1-5, 7-16, 18-27, and 29-30 are presented for examination.

35 U.S.C. §102(e) Rejection

Claims 1-30 stand rejected under 35 U.S.C. §102(e) as being anticipated by Sih et al. (U.S. Patent No. 6,606,700). Applicant submits that the present claims are patentable over Sih.

Sih discloses a digital signal processor architecture that is designed to speed up frequently-used signal processing computations, such as FIR filters, correlations, FFTs, and DFTs. The architecture uses a coupled dual-MAC architecture and attaches a dual-MAC coprocessor onto it in such a way as to achieve an increase in processor capability. (Sih at col. 1, ll. 49-55.)

Claim 1, as amended, recites:

> A method comprising:
> receiving input data by an execution unit; and
> performing, by the execution unit using a plurality of multiply-accumulate units in the execution unit, a plurality of current multiply-accumulate operations on the received input data;
> wherein the performing a current multiply-accumulate operation includes:
> multiplying the received input data with a multiplier in the execution unit;
> adding an output from the multiplier with another value using an adder in the execution unit; and
> storing an output of the adder and providing the another value to the adder using an accumulator in the execution unit; and

wherein the performing is to implement a finite impulse response filter with the received input data comprising one or more tap coefficients and one or more input data samples and with accumulated data in the accumulator comprising one or more output data samples.

Applicant submits that Sih does not disclose or suggest performing a plurality of multiply-accumulate operations to implement a finite impulse response filter with received input data comprising one or more tap coefficients and one or more input data samples and with accumulated data in an accumulator comprising one or more output data samples, as recited by amended claim 1. Sih discloses a digital signal architecture that is designed to speed up frequently-used digital signal processing computations, such as FIR filers. (See Sih at Abstract.) However, Sih does not disclose the level of detailed implementation disclosed in the features of claim 1. Specifically, there is no disclosure or suggestion in Sih of implementing a finite impulse response filter via multiple-accumulate operations *with received input data comprising one or more tap coefficients and one or more input data samples and with accumulated data in an accumulator comprising one or more output data samples*. Therefore, claim 1 is patentable over Sih.

Claims 2-5 and 7-9 depend from claim 1 and include additional limitations. Therefore, claims 2-5 and 7-9 are also patentable over Sih.

Independent claims 10 and 21 also recite, in part, performing a plurality of multiply-accumulate operations to implement a finite impulse response filter with received input data comprising one or more tap coefficients and one or more input data samples and with accumulated data in an accumulator comprising one or more output data samples. As discussed above, Sih does not disclose or suggest such a feature. Therefore, claims 10 and 21, as well as their respective dependent claims, are patentable over Sih for the reasons discussed above with respect to claim 1.

Applicant respectfully submits that the rejections have been overcome and that the claims are in condition for allowance. Accordingly, applicant respectfully requests the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Applicant respectfully petitions for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17(a) for such an extension.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: February 21, 2006

Ashley R. Ott
Reg. No. 55,515

12400 Wilshire Boulevard
7th Floor
Los Angeles, California 90025-1026
(303) 740-1980